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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,284	11/26/2001	Sang Ick Lee	CU-2636 VE	8830

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EXAMINER	
PHAM, THANH V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,284	LEE ET AL.	
	Examiner	Art Unit	
	Thanh V Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2004 and 06 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. attached herewith.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Based on the interview on 09/24/04, the Finality of the Office action mailed 09/16/04 is withdrawn.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/12/04 has been entered.

Response to Amendment

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-3, 5-6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art in combination with Maniar et al. U.S. Patent No. 5,356,833 and the following.

The applicants' admitted prior art as explained in figures 1 and 2 and the background of the invention has a method of forming a gate in a semiconductor device having a non-linear top profile *(that is substantially the same as the detailed description*

of the preferred embodiments referring to FIG. 3A to 3F), the method comprising the steps of:

forming a dummy gate insulating layer 2 on a semiconductor substrate 1 having a field oxide layer isolating the device (not shown, page 3, lines 13-14);

depositing a dummy gate polysilicon layer 3 and a hard mask layer 4 on the dummy gate insulating layer 2 sequentially;

patterning the hard mask 4 into a mask pattern 4a and patterning the dummy gate polysilicon layer 3 and the dummy gate insulating layer using the mask pattern as an etch barrier, creating a plurality of patterned dummy gate polysilicon and insulating layers each having sidewalls, wherein the patterned dummy gate polysilicon and insulating layers are formed on the semiconductor substrate and on the field oxide layer;

forming spacers 6 at the sidewalls of the patterned dummy gate polysilicon 3 and insulating layers;

depositing an insulating interlayer 7 on the resultant structure 5 after forming the spacers 6;

exposing a surface of the patterned dummy gate polysilicon and insulating layers by carrying out an oxide layer CMP process, page 4, line 14, using a first selection ratio sufficient to polish the insulating layer but insufficient to polish the patterned dummy gate polysilicon and insulating layers;

forming a damascene structure by removing the patterned dummy gate polysilicon and insulating layers using the insulating interlayer as another etch barrier, fig. 1D, page 4, lines 15-16 and page 5, lines 1-3;

depositing a gate insulating layer 8 and a gate metal layer 9 on the entire surface of the semiconductor substrate having the damascene structure, fig. 1E; and

exposing a surface of the insulating interlayer by carrying out a metal chemical mechanical polishing process using a second selection ratio sufficient to polish the metal layer but insufficient to polish the insulating interlayer.

The metal CMP uses slurry for a metal layer, page 13, lines 6-19.

In the description of applicant's admitted prior art the applicant does not state the thickness of the dummy gate polysilicon layer or the insulating interlayer, the polishing selection ratios between the insulating interlayer and the dummy gate polysilicon layer is over 20 or the gate metal layer is over 50, **the using of CeO_2** and its pH between 3 and 11 in the insulating interlayer CMP and the pH between 2 and 7 of the slurry in the metal layer CMP.

The Maniar et al. reference discloses use of CeO_2 as slurry in CMP oxide removal process in the variation of topologies with a pH in a range of about 2-5 or the pH outside the range may be used (col. 4, lines 23-40 and col. 5, line 57 to col. 6, line 29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the known CeO_2 as the slurry in the known CMP process in the structure of applicant's admitted prior art as CeO_2 would be selected in accordance with the variation of topologies structure in the applicant's admitted prior art.

Moreover, with the confirmation of applicants' argument that the CMP slurry disclosed in the cited Maniar et al. reference is one of a number of materials well known in the art (the Remark, paper #7, page 3, lines 1-2, filed 12/13/02), the recited selection ratios would be obtained in the process of the combination because the same known materials are treated in the same manner as in the instant invention. The *"result in a structure wherein the heights of the resulting metal gates on the field oxide layer are at substantially the same height as the resulting metal gates on the active area"* is provided by the protection of the same material sidewall spacers. The 'wave-like' profile of the top of the gates is inherently formed.

Choice of 1,300 to 2,000 angstroms for the gate layer and 4,000 to 5,000 angstroms for the interlayer to achieve particular device properties would have been a matter of routine optimization because the thickness is known to affect device properties and would depend on the desired device density on the finished wafer and the desired device characteristics.

Response to Arguments

5. Applicant's arguments filed 04/06/04 have been fully considered but they are not persuasive.

6. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir.

1986). In this instance, as in the previous Remarks, applicant repeatedly argues on the conventional CMP in the applicant's admitted prior art (page 5's first and second full paragraphs, page 6's first and third full paragraphs, page 7's first full paragraph and page 9's last paragraph) and Maniar et al.'s selectivity of 1:1 in example 1 (page 7's second full paragraph and page 9). The combination of the rejection uses the structure of applicant's admitted prior art not the conventional CMP on that structure, and Maniar et al.'s use of CeO_2 as slurry in CMP in the variation of topologies not just in example 1. The same known materials are treated in the same manner as in the instant invention would yield a *"result in a structure wherein the heights of the resulting metal gates on the field oxide layer are at substantially the same height as the resulting metal gates on the active area"*. The 'wave-like' profile of the top of the gates is inherently formed when CeO_2 is used in CMP on the provided structure with the protection of the same material sidewall spacers. *(Note: This passage is partially extracted from the Advisory action mailed 01/30/04 and the Final action mailed 10/07/03).*

7. In response to applicant's argument in the second full paragraph of page 6, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

8. In response to applicant's argument that the present invention is non-obvious over applicant's admitted prior art in view of the lack of teaching of Maniar et al., the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

9. In response to applicant's argument that the teaching away by Maniar et al. from such a combination, Maniar et al. discloses forming members 91-93 "using the aqua 'regia' solution previously described" col. 8, lines 19-24, to have a non-planar topology as in fig. 9, e.g., "the present invention may be used with any semiconductor substrate including silicon, ... , used with devices including MOSFET, ... , volume changes due to the reaction may need to be taken into account", col. 6, lines 10-28, "the intermetallic layer does not have to be very conformal", col. 10, lines 17-18. Those recognized facts by Maniar et al. are utilized to modify the applicant's admitted prior art structural gates in order to obtain the MOSFET recited in the claims of this application to prevent the gates being decapitated. The Maniar et al. reference discloses use of CeO2 as slurry in CMP process in the variation of topologies with a PH in a range of about 2-5, the PH outside the range may be used (col. 4, lines 23-40 and col. 5, line 57 to col. 6, line 29). The recited selection ratios (the polishing selection ratios between the insulating interlayer and the dummy gate polysilicon layer is over 20 or the gate metal layer is over 50) would be obtained because the same materials are treated in the same manner as in

the instant invention. *(Note: These two passages are extracted from the Advisory action mailed 01/30/04).*

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TvP
10/18/04

George Fourson
Primary Examiner